# VLSI TECHNOLOGY & DESIGN
(ELECTIVE – I)

**Course Code:**15EC2202

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**Prerequisites:**
Electronics Devices and Circuits, Switching Theory and Logic Design.

**Course Outcomes:** Student will be able to

**CO1:** Distinguish different IC technologies and analyze basic electrical properties of MOS, CMOS & Bi-CMOS circuits.
**CO2:** Draw layouts for logic gates.
**CO3:** Analyze the concepts of alternate gate circuits, interconnect delays, Gate and Network testing.
**CO4:** Outline the concept of memory cells, clocking disciplines, power optimization, design validation & testing.
**CO5:** Acquire knowledge of floor-plan methods, High level synthesis, CAD systems and methodologies for chip design.

**UNIT-I** (10-Lectures)

**BASIC ELECTRICAL PROPERTIES OF MOS, CMOS & BICMOS CIRCUITS:**

Review of Microelectronics: (MOS, CMOS, Bi CMOS) Technology trends and projections. Ids-Vds relationships, Threshold voltage $V_t$, $G_m$, $G_{ds}$ and $W_o$, Pass Transistor, MOS, CMOS & Bi-CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

**UNIT-II** (10-Lectures)

**LAYOUT DESIGN AND TOOLS:**

Transistor structures, Wires and Vias, Scalable Design rules, Layout Diagrams for NMOS and CMOS Inverters and Gates, Layout Design tools.

**UNIT-III** (10-Lectures)

**LOGIC GATES &COMBINATIONAL LOGIC NETWORKS:**

Static complementary gates, switch logic, Alternative gate circuits, low power gates, Resistive and Inductive interconnect delays. Layouts, Simulation, Network delay, interconnect design, power optimization, Switch logic networks, Gate and Network testing.

**UNIT-IV** (10-Lectures)

**SEQUENTIAL SYSTEMS:**

Memory cells and Arrays, clocking disciplines, Design, power optimization, Design validation and testing.

**UNIT-V** (10-Lectures)

**FLOOR PLANNING &CHIP DESIGN:**

Floor planning methods, off-chip connections, High-level synthesis, Architecture for low power, SOCs and Embedded CPUs, Architecture testing. Introduction to CAD systems (algorithms) and chip design - Layout Synthesis and Analysis, Scheduling and binding, Hardware/Software Co-design, chip design methodologies- A simple Design example.

**TEXTBOOKS:**

1. Kamran Eshraghian, Eshraghian Dougles and A. Pucknell, "*Essentials of VLSI circuits and systems*", 3rd Edition, PHI, 2005.
2. Wayne Wolf, "*Modern VLSI Design*", Pearson Education, 3rd Edition, 2008.

**REFERENCES:**

1. Weste and Eshraghian, "*Principles of CMOS VLSI Design*", Pearson Education, 3rd Edition, 1999.
2. Fabricius, "*Introduction to VLSI Design*", MGH International Edition, 1990.
3. Baker and Li Boyce, "*CMOS Circuit Design, Layout and Simulation*", PHI, 2004.